REMARKS

Claims 1-9 have been examined.

The Examiner maintains, and makes final, the rejection of claims 1-7 under 35 U.S.C. § 102(b) as being anticipated by Toyoda et al. (JP 405166965A), and the rejection of claims 8 and 9 under 35 U.S.C. § 103(a) as being obvious from Toyoda. For the following reasons, Applicant traverses these rejections.

Independent claim 1 recites, *inter alia*, that at least one through hole is formed in the signal line and an inner wall of said through hole is not electrically connected to said signal line and said ground plate. In addition, independent claim 2 includes at least one hole formed in the ground plate and an inner wall of said through hole is not electrically connected to said signal line and said ground plate. Further, independent claim 5 includes at least one hole formed in both the signal line and the ground plate and an inner wall of said through hole is not electrically connected to said signal line and said ground plate.

That is, in each of independent claims 1, 2, and 5, at least one hole is formed in either the signal line or the ground plate to increase the characteristic impedance between two adjacent signal lines or between one signal line and the ground plate. Moreover, in each of claims 1, 2, and 5, the inner wall of the through hole is not electrically connected to the signal line and the ground plate.

The Examiner alleges that Toyoda discloses an insulating board or ground plate 44 and a signal line 46 controlled in specific impedance by holes formed in the signal line, as evidenced by Figures 1 and 3, reference numeral 48. Applicant respectfully disagrees.

Contrary to the claimed invention, Toyoda neither discloses, teaches, nor suggests forming holes in the signal line or ground plate to increase the characteristic impedance. Instead, Toyoda merely discloses an insulating board 44, which includes through-holes 56, 58, wherein ground patterns 48, 52 and signal lines 46, 50 are formed on the insulating board 44. That is, the through-holes are formed in the insulating board 44, not in the signal lines or ground plates. Accordingly, neither the ground patterns 48, 52 nor the signal lines 46, 50 are formed with at least one hole for increasing the characteristic impedance, as claimed by Applicant.

Moreover, contrary to the claimed invention, the through holes 56, 58 of Toyoda contain conductors that electrically connect the front-face side signal lines and ground patters with the rear-face side signal lines and ground patterns.

Accordingly, Applicant submits that Toyoda neither discloses, teaches, or suggests all of the recitations of independent claims 1, 2, and 5, and therefore, these claims are neither anticipated by, nor obvious from, the Toyoda reference.

In addition, claims 3, 4, and 6-9 also are patentable over Toyoda at least by virtue of their dependency from claims 1 and 5, respectively.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Twice Amended) A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure comprising a signal line and a ground plate, wherein at least one through hole is formed in said signal line, and an inner wall of said through hole is not electrically connected to said signal line and said ground plate.

2. (Twice Amended) A semiconductor integrated circuit comprising a signal transmission line patterns of a microstrip structure comprising of a signal line and a ground plate, wherein at least one through hole is formed in said ground plate, and an inner wall of said through hole is not electrically connected to said signal line and said ground plate.

5. (Twice Amended) A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure comprising a signal line and a ground plate, wherein at least one hole is formed in both of said signal line and said ground plate, and an inner wall of said hole is not electrically connected to said signal line and said ground plate.